UNIVERSITY OF CAPE TOWN
IYUNIVESITHI YASEKAPA • UNIVERSITEIT VAN KAAPSTAD

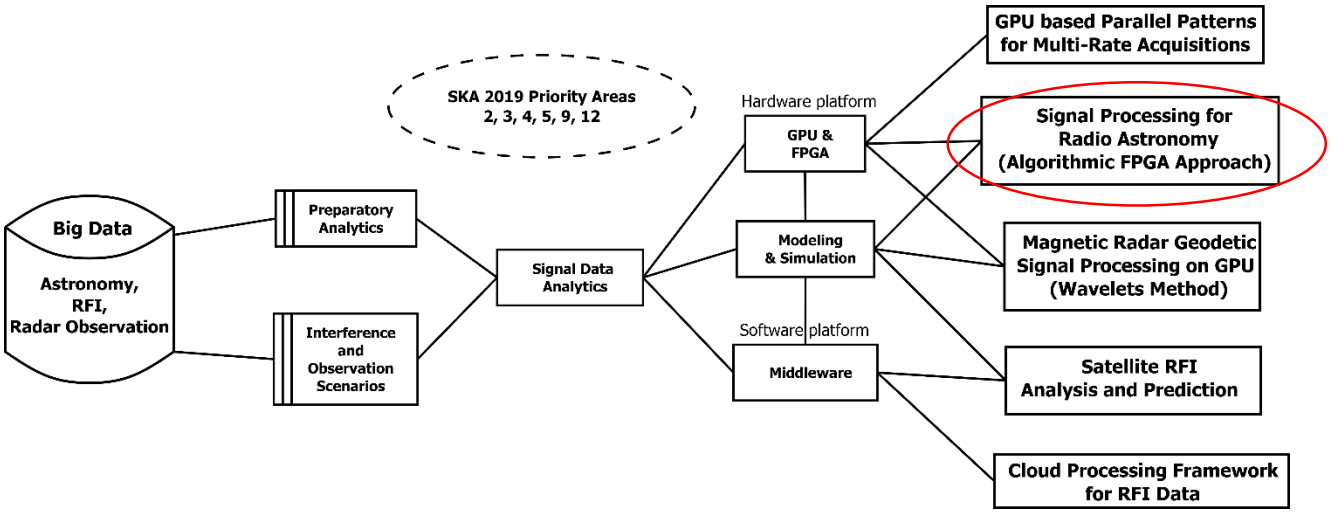
Section A / Attachment 3

Title:
OptiSDR radio astronomy enhancements for GPU-based Parallel Patterns for Multi-Rate Acquisitions

Section A: Overview of the Research Project Proposal

1. **Academic level of research project:** Master's
2. **Broad field of research:** Engineering
3. **Title of the research project:** OptiSDR radio astronomy enhancements for GPU based Parallel Patterns for Multi-Rate Acquisitions
4. **Research project abstract/summary (max 250 words):** A basic parallel processing framework and platform is in place at the Radar Remote Sensing Group. The student will enhance capability of this system by embedding parallel computing patterns, memory access patterns and signal processing routines. Additional task is to support real-time acquisition and processing capability by integrating ROACH or Pentek DAQ system.

This proposal arches to our bigger project view, shown below, in the skill development areas of FPGA/GPU hardware, instrumentation and data analytics that are related to the SKA requirements.



Section B: Supervisor Details

1. Primary supervisor's details
Title and full name: **Dr. Simon Winberg**
b. Name of South African or SKA Partner Country university at which the primary supervisor is a permanent academic staff member : **South Africa**
c. Email address and/or contact telephone number (please note that in the event this project is approved, these contact details will be made available to students awarded SARAO postgraduate bursaries): **Email:** Simon.Winberg@uct.ac.za **Tel: +27 (0)21 650 2793**
d. Supervision of postgraduate students – please provide the details of all the previous and current postgraduate students supervised. Please provide the information in table format, as shown below.

Students current supervised and graduated

This section lists students currently supervised and graduated since 2013.

Doctoral Students (since 2013)

Name of student	Nationality	Date started Doctoral Degree (Month and Year)	Date completed / will complete Doctoral Degree (Month and Year)	Title of Research Project / Thesis	Co-Supervisor
Mr Lerato Mohapi (graduated)	Lesotho	1-Feb-2014	18 October, 2017	A domain specific language for facilitating automatic parallelization and placement of SDR patterns into heterogeneous computing architectures	Michael Inggs (UCT)
Mr Danish Arif	Pakistan	24-Feb-2015	December 2019	Angle Independent Face Recognition for High Value Targets	
Mr John-Philip Taylor	South Africa	1-Mar-2015	December 2019	Alcha: Architectural Level Computational Hardware Abstraction: A New Programming Language for FPGA Projects	
Mr Lekhobola Tsoeunyane	Lesotho	15-Feb-2016	April/June 2019	Framework for integration of SDR applications using a DSL with SDF-AP dataflow models	Michael Inggs (UCT)
Mr Joseph Wamicha	Kenya	20-Feb-2017	December 2019	Investigation of a Low-Powered Mechatronic System to Enhance Power Generation of a PV Solar Array	
Mr Zeeshan Aleem	Pakistan	15-Feb-2016	December 2018	Development and Improvement in Control and Miscellaneous Aspects of Impedance Source Inverters and Converters	Moin Hanif (Dublin Institute of Technology)

ii. Masters Students

Name of student	Nationality	Date started Master's Degree (Month and Year)	Date completed / will complete Master's Degree (Month and Year)	Title of Research Project / Thesis	Co-Supervisor
Mr Bradlee Wilson (graduated)	South Africa	Feb 2016	June 2018	Autonomous RGB-Depth Sensing 3D mapping robot	Daniel O'Hagan (UCT)
Ms Aphiwe Hotele (graduated)	South Africa	Feb 2016	December 2017	Environmental Monitoring Predictor: A case study of	

				the Meerkat Science Data Processor Imager	
Ms. Mpati Boleme (graduated)	Lesotho	Feb 2015	June 2016	Rhino streaming interface for Gnu Radio with performance testing case studies	
Mr Israel Tshililo (graduated)	South Africa	Feb 2015	December 2016	Parallelization of galaxy formation modelling algorithms	Catherine Cress (CHPC / UWC)
Mr Wesley New (graduated)	South Africa	Feb 2015	December 2016	Python Based FPGA Design-flow	Michael Inggs (UCT)
Mr Pius Mugagga (graduated)	Uganda	June 2013	December 2015	Human hearing augmentation device	
Mr Lekhobola Tsoeunyane (graduated)	Lesotho	Feb 2015	December 2015	RHINO SDR Blocks	Michael Inggs (UCT)
Ms Valerie Chiriseri (graduated)	Zimbabwe	Feb 2013	December 2014	RHINO API Cluster Control Management System	
Mr Shaun Katz (graduated)	South Africa	Feb 2012	June 2013	RadiO Modelling Environment (ROME)	
Mr Karthik Rajeswaran (graduated)	United Arab Emirates	Feb 2012	December 2013	Losless compression of SKA Data Sets	
Mr Shaylin Chetty	South Africa	2018		A Heterogeneous System Architecture Based Image Processing Framework	
Mr Lindokuhle Biyas	South Africa	2017		SKA RFI Data Store and Remote Access Processing System	
Mr Josiah Shumba	Zimbabwe	2018		Cognitive Radio Wireless Sensor Network (CRWSN) Framework	
Mr Luckmore Magwa	Zimbabwe	2018		Spectrum Sensing to Characterising Interference from Base Stations	
Mr Balone Ndaba	Lesotho	2016		OpenCL SDR Signal Steam	

				Processing Framework for the Xeon Phi	
Mr Khobatha Setetemela	Lestho	2018		Evaluation of High Level Tool-Flows for Rapid Prototyping of Software-defined Radios on FPGAs	
Mr Mbongeni Bhebhe	Zimbabwe	2018		Characterizing Noise from Narrow Band Internet of Things (NBIoT) for certain sensor nets	
Mr Yemeli Tasse	Cameroon	2017		Dynamic Signal Conditioning System for FPGA-based sampling systems	
Mr Bradley Kahn	South Africa	2016		Parameter control system for RHINO signal timing and sampling	
Mr Daniel Flowers	South Africa	2017		Stacked Denoising Autoencoder For Self-Organizing Maps	

2. Co-supervisor / Research Supervisor's details
a. Dr. Syed Muhammad Yaseen Zaidi
b. University of Cape Town
c. yaseen.zaidi@ieee.org / 021 650 2792
d. Supervision

The following students were supervised/co-supervised during co-supervisor's tenure at the Cape Peninsula University of Technology.

ii. Masters Students

Primary Supervisor

Name of student	Nationality	Date started Masters (Month and Year)	Date completed / will complete Master's Degree (Month and Year)	Title of Research Project / Thesis	Co-Supervisor
Caleb Hillier	South Africa	March, 2017	-	A System on Chip (SoC) based Error Detection And Correction (EDAC) Implementation for Nanosatellites	Robert van Zyl

Co-supervisor

Name of student	Nationality	Date started Masters (Month and Year)	Date completed / will complete Master's Degree (Month and Year)	Title of Research Project / Thesis	Primary Supervisor
Kanyisa Sipho Mtshemla (graduated)	South Africa	January, 2015	September, 2017	Mission design of a CubeSat constellation for in-situ monitoring applications	Robert van Zyl

Research Supervisor

Name of student	Nationality	Date started Masters (Month and Year)	Date completed / will complete Master's Degree (Month and Year)	Title of Research Project / Thesis	Co-Supervisor
Inge Chleo Pearce	South Africa	January, 2015	September, 2017	Magnetic Hardware In-The-Loop Simulator for a Nanosatellite	Robert van Zyl, Gerard Orjubins

Joel Biyoghe	Democratic Republic of Congo	January, 2015	-	Implementation of Quadrature Phase Shift Keying (QPSK) Modulation in FPGA for High Data Rate Nanosat Missions	Robert van Zyl, Yves Blanchard
Lilie Nally Leopold	Namibia	January, 2014	-	Design and Implementation of a C-Band Downconverter Receiver	Robert van Zyl, Francois Visser

Students significantly helped in part selection, developing a focused proposal, test and measurements, publications and in thesis review:

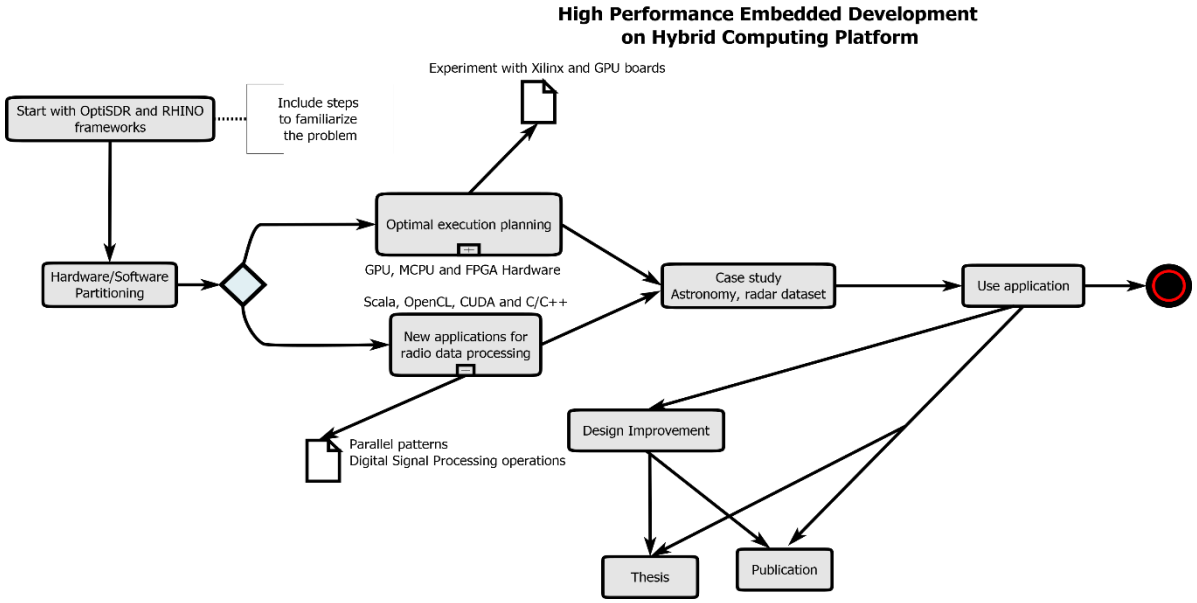
Name of student	**Nationality**	**Date started Masters (Month and Year)**	**Date completed / will complete Master's Degree (Month and Year)**	**Title of Research Project / Thesis**	**Co-Supervisor**
Lusanda Mdibi	South Africa	February, 2016	November, 2018	A Land based HF Transmitter for Ionospheric Propagation Studies Using SuperDARN Radars	Robert van Zyl, Mike Kosch (SANSA Hermanus)
Verena K. Naftali	Namibia	February, 2016	November, 2018	Implementation of Reverberation Chamber for Electromagnetic Compatibility Measurements	Robert van Zyl, Gerard Orjubin
Pamela Mvouezolo	Democratic Republic of Congo	July, 2015	-	On Improvement of the Reverberation Chambers with Two Stirrers	Robert van Zyl, Gerard Orjubin

Section C: Full Research Project Proposal

1. **Scientific Merit:** Current large dataset processing capability is limited by a few parallel patterns and signal processing routines.
2. **Feasibility:** We propose to utilize high performance parallel embedded computing platform currently available at the group. This is a heterogeneous architecture that can be programmed at varying abstraction levels rendered by VHDL, Python, OpenCL and CUDA on either FPGAs, GPUs or MCPUs or combinations thereof. We have a software framework, called OptiSDR, that supports such heterogeneous development. This project therefore proposes to extend the OptiSDR framework to DSP process the radio astronomy, RFI, radar or remote sensing data as huge chunks. The framework would select the most suitable device (FPGA, GPU or MCPU) in terms of cache memory access, parallelization and other hardware/software resources, and

based on data structure and correlation of samples. This will speed up the analysis of data and object patterns can be outlined for the experts to reason about the observations. At the same time the student will learn advanced skills of digital signal processing on high-end computing platforms.

The detail of the project is shown in figure below.



3. Link to SARAO priority areas: This project connects to three areas: 2 i.e., signal processing using FPGA and GPU platforms, area 4 i.e., big data and development of hardware and middleware platforms and area 9 that relates to geodesy.

4. Student profile: BSc/BEng degree in electronics or electrical engineering from ECSA recognized university or equivalent. Background (coursework, thesis /project, internship or job experience) in signal processing will be highly useful along with good analytical and problem solving skills. Graduates of Computer Science with strong programming / computational skills may also fit.

Section D: Signatures

Simon Winberg
(Primary supervisor)

Thursday, 30 August 2018 Thursday, 30 August 2018